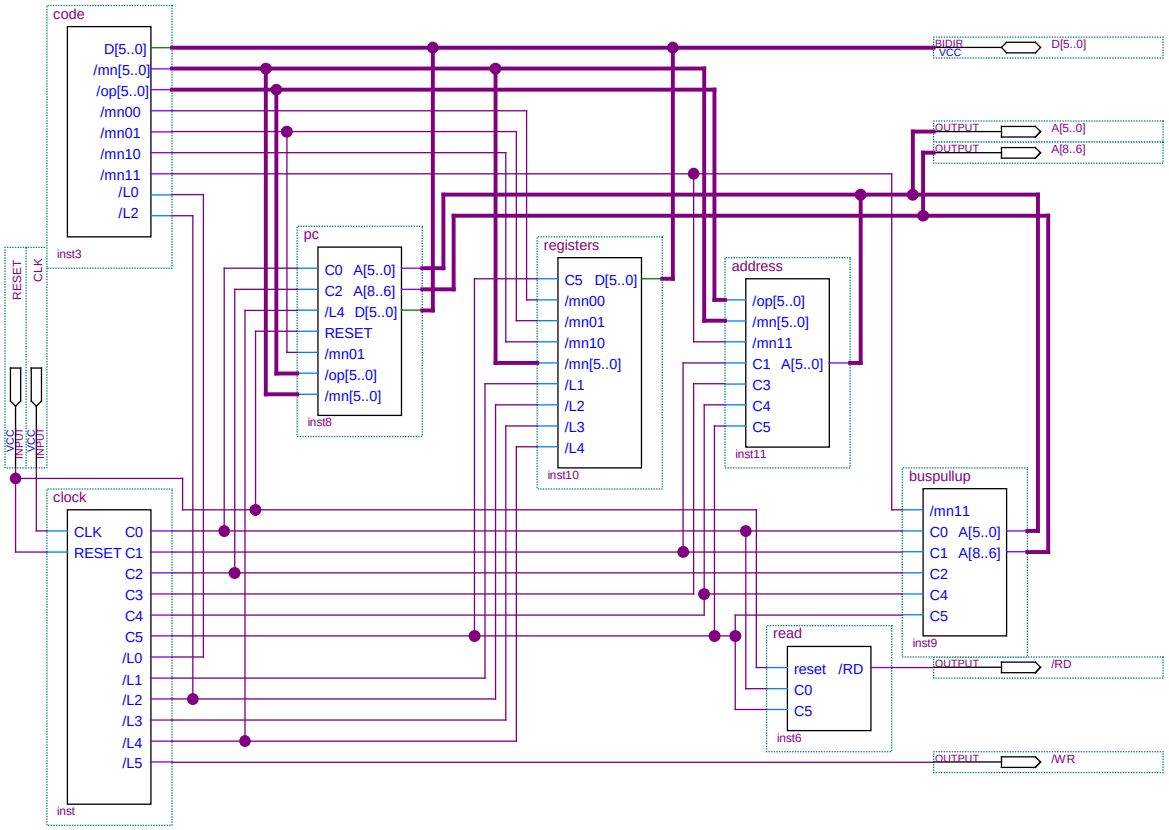
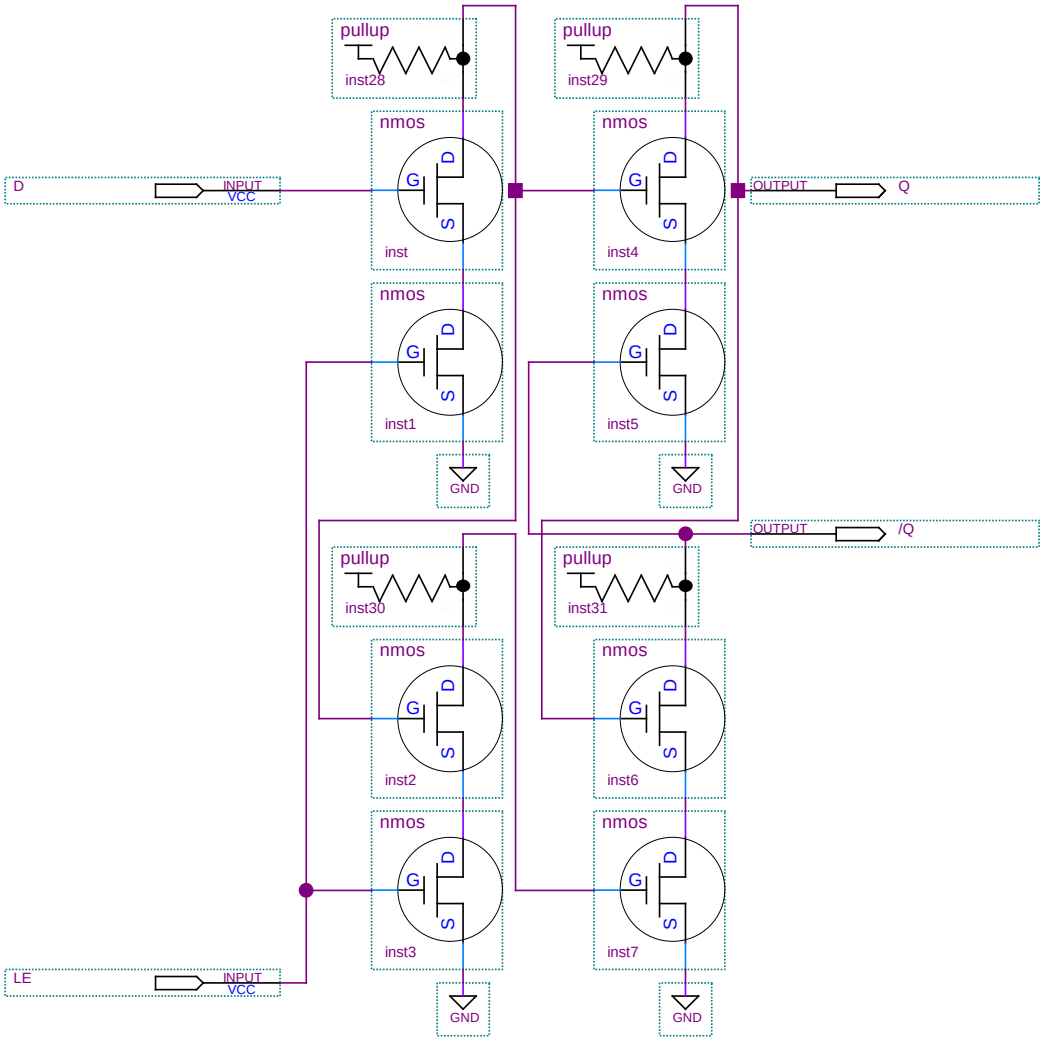
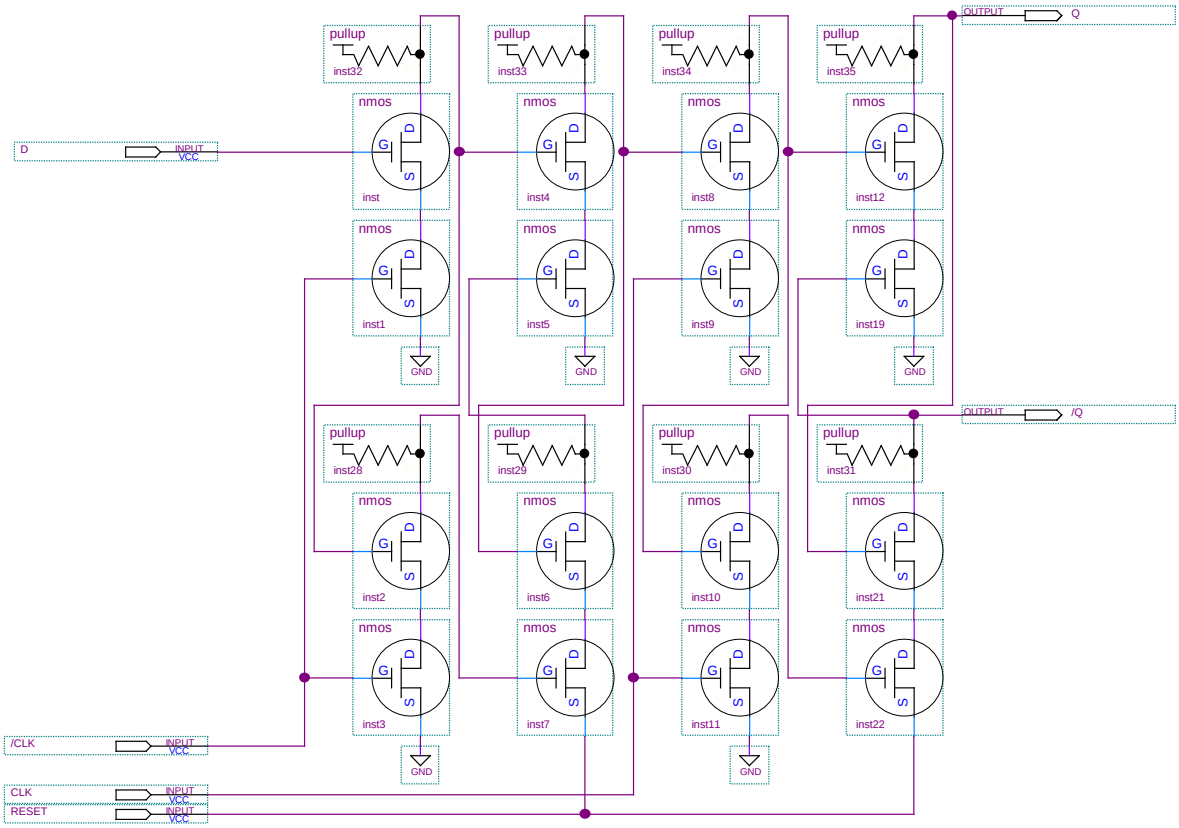
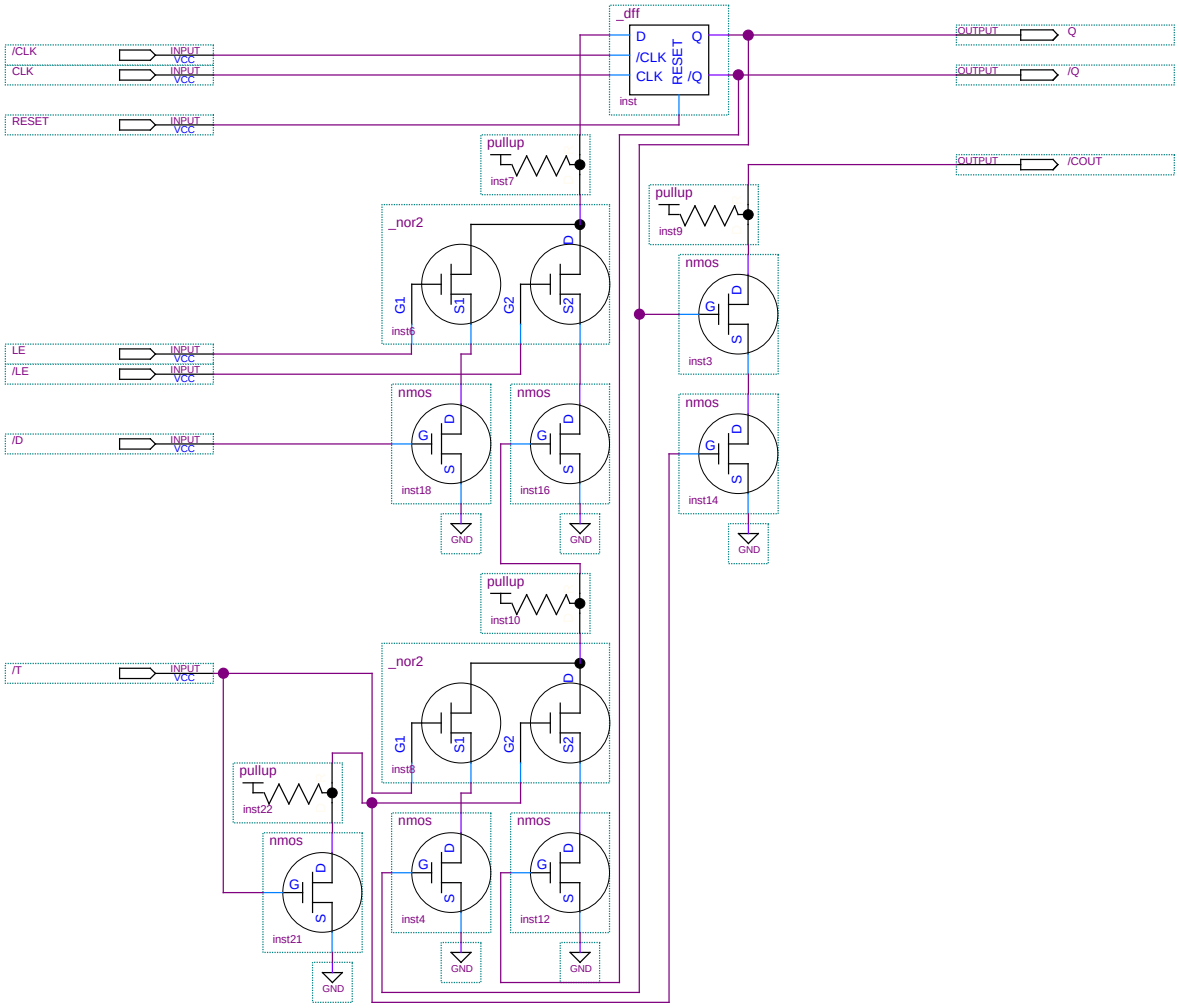
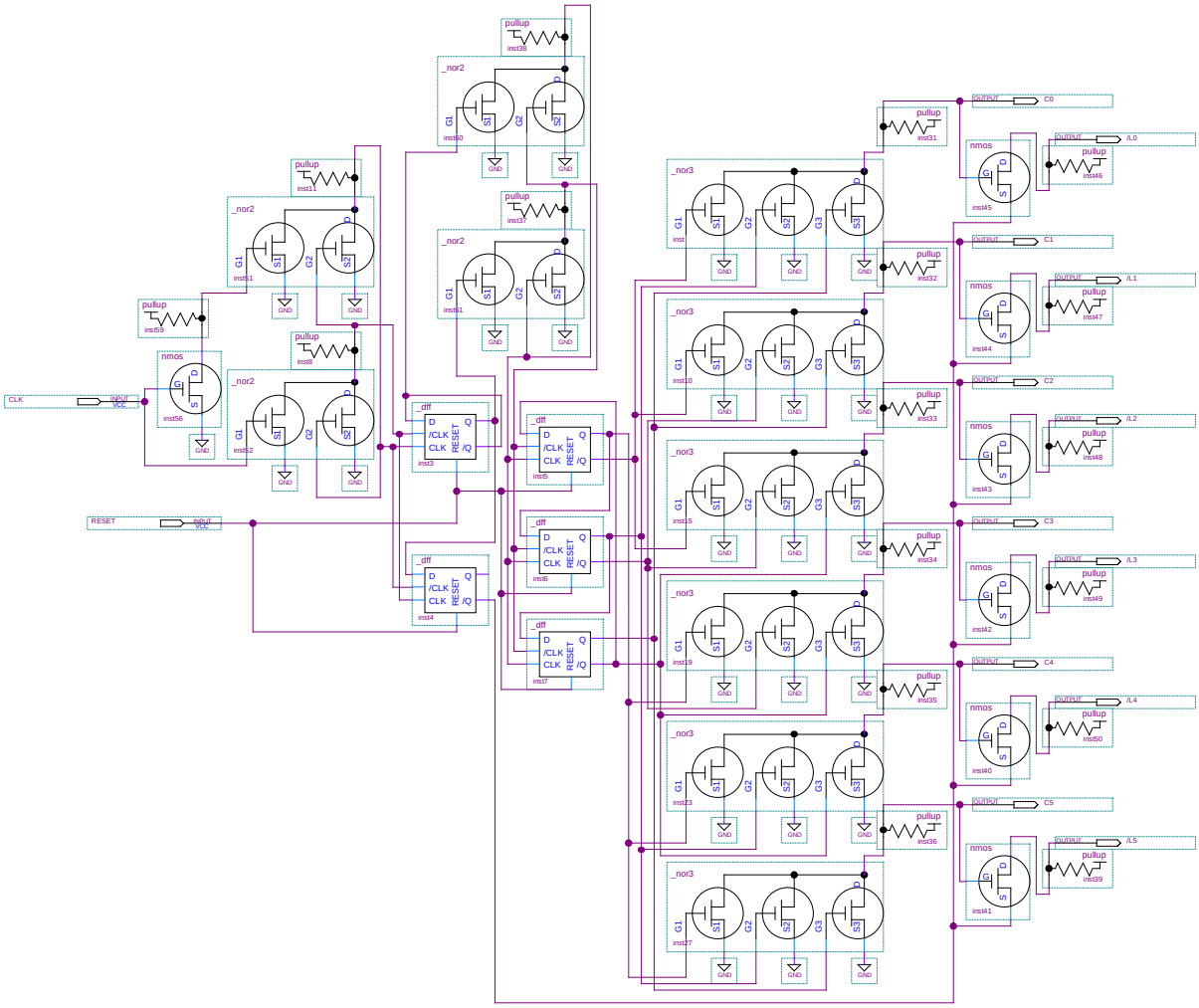
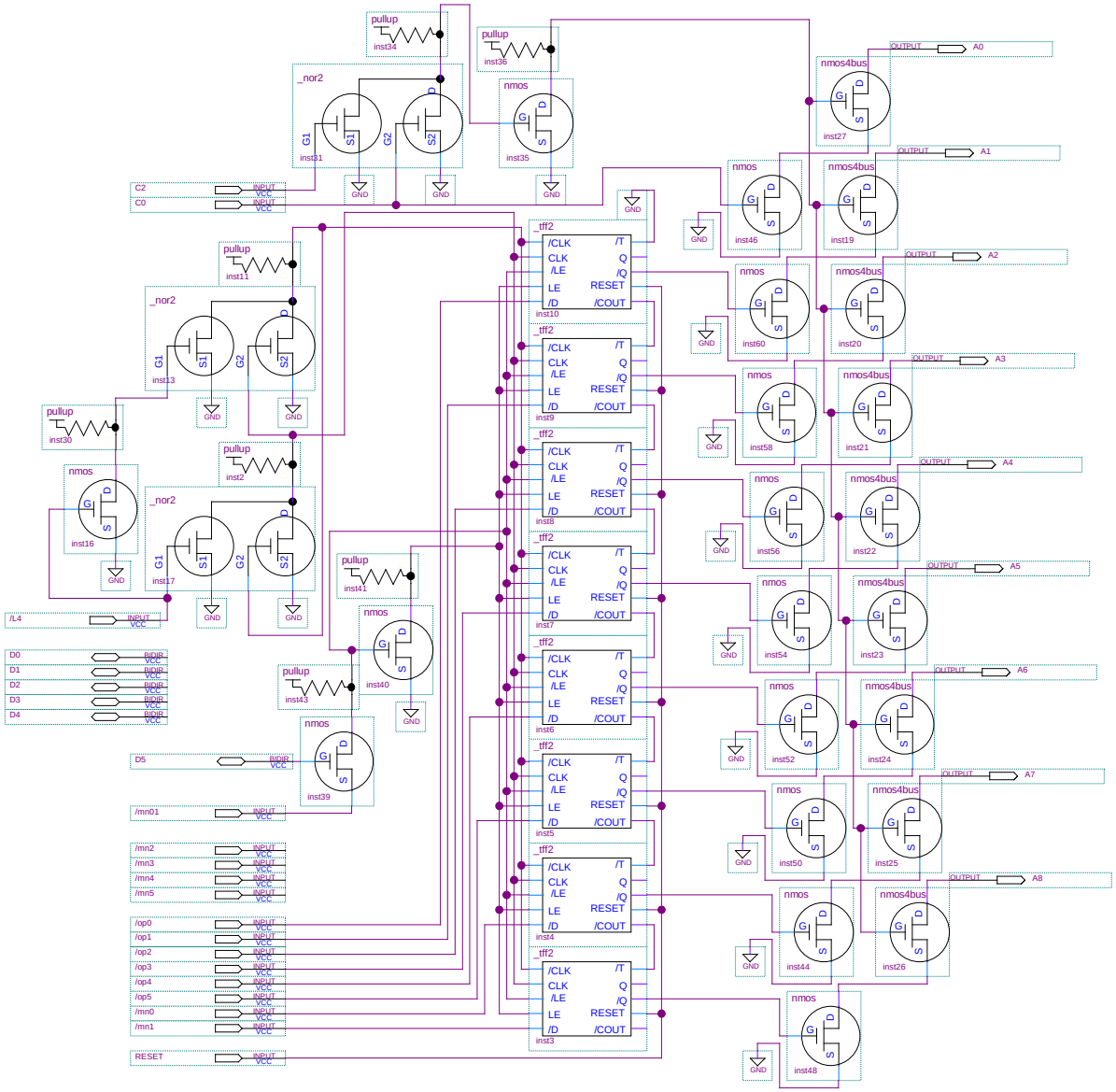

code
D[5..0]
/mn[5..0]
/op[5..0]
/mn00
/mn01
/mn10
/mn11
/L0
/L2
inst3
RESET
CLK
VCC
INPUT
INPUT
pc
C0 A[5..0]
C2 A[8..6]
/L4 D[5..0]
RESET
/mn01
/op[5..0]
/mn[5..0]
inst8
registers
C5 D[5..0]
/mn00
/mn01
/mn10
/mn[5..0]
/L1
/L2
/L3
/L4
inst10
address
/op[5..0]
/mn[5..0]
/mn11
C1 A[5..0]
C3
C4
C5
inst11
BIDIR
VCC
D[5..0]
OUTPUT
A[5..0]
OUTPUT
A[8..6]
buspullup
/mn11
C0 A[5..0]
C1 A[8..6]
C2
C4
C5
inst9
clock
CLK C0
RESET C1
C2
C3
C4
C5
/L0
/L1
/L2
/L3
/L4
/L5
inst
read
reset /RD
C0
C5
inst6
OUTPUT
/RD
OUTPUT
/WR

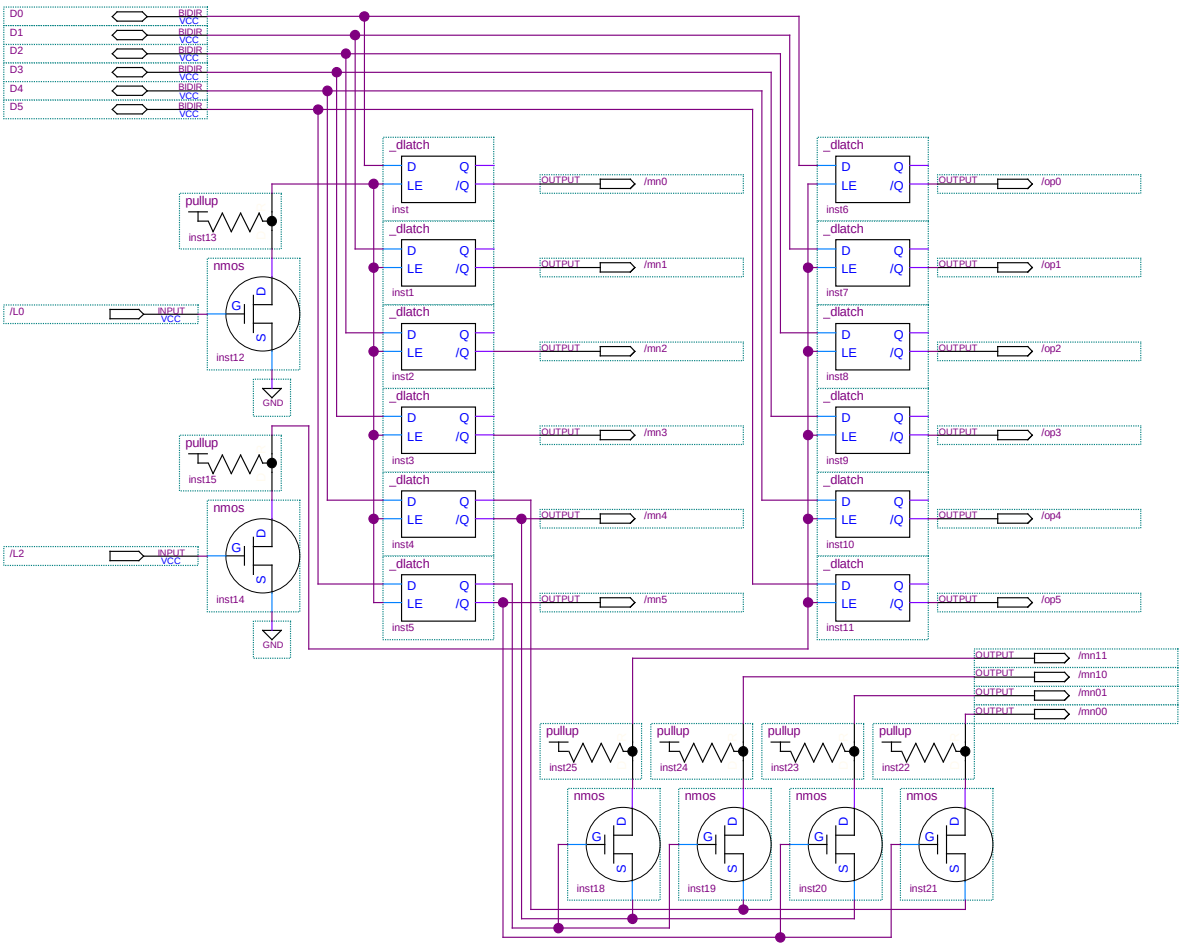

pullup
inst28
pullup
inst29
nmos
inst
nmos
inst4
D
INPUT
VCC
OUTPUT
Q
nmos
inst1
nmos
inst5
GND
GND
OUTPUT
/Q
pullup
inst30
pullup
inst31
nmos
inst2
nmos
inst6
nmos
inst3
nmos
inst7
LE
INPUT
VCC
GND
GND

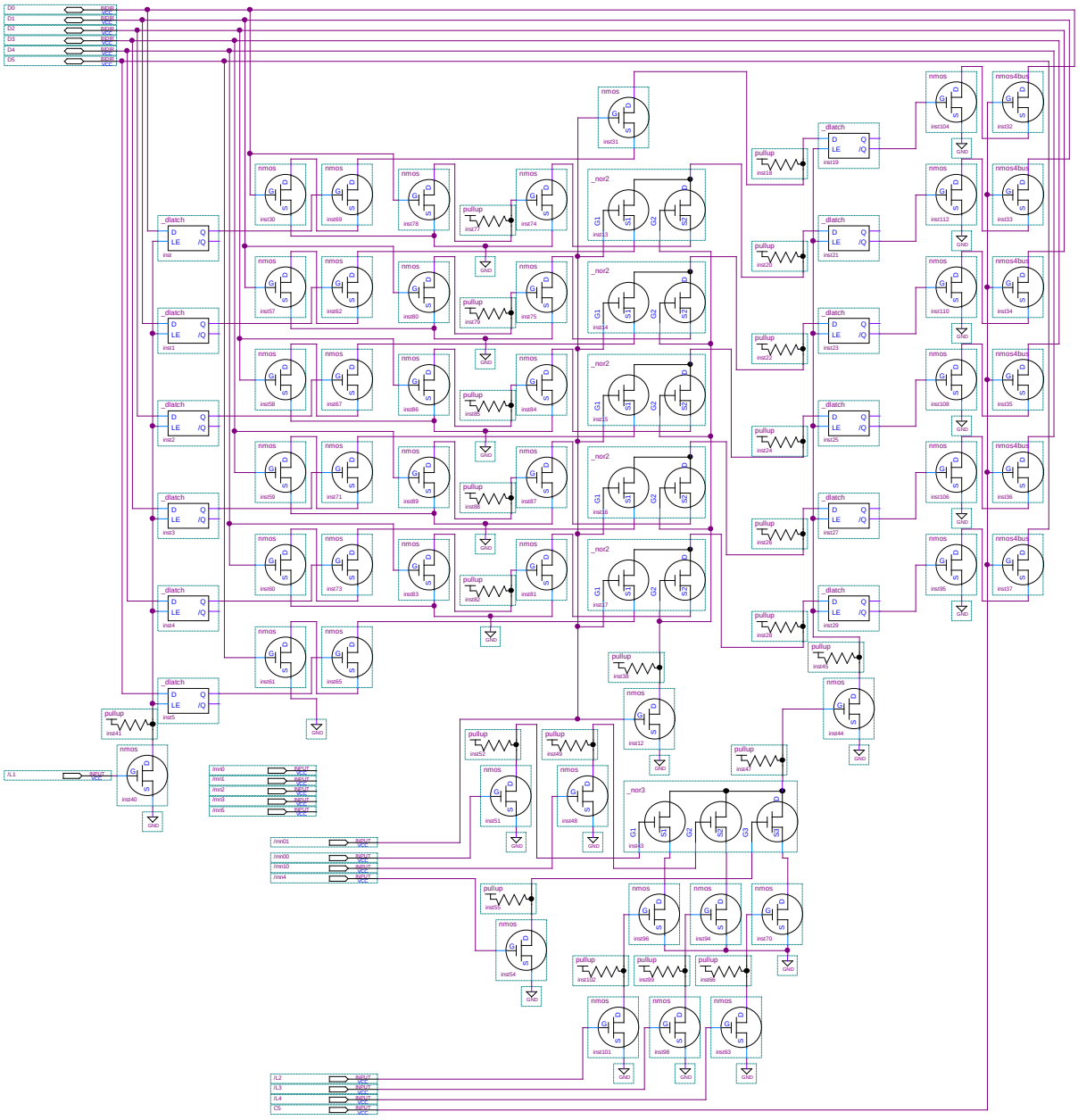

D
INPUT
VCC
/CLK
INPUT
VCC
CLK
INPUT
VCC
RESET
INPUT
VCC
OUTPUT
Q
OUTPUT
/Q
pullup
inst32
pullup
inst33
pullup
inst34
pullup
inst35
pullup
inst28
pullup
inst29
pullup
inst30
pullup
inst31
nmos
inst
inst1
inst2
inst3
inst4
inst5
inst6
inst7
inst8
inst9
inst10
inst11
inst12
inst19
inst21
inst22
G
D
S
GND

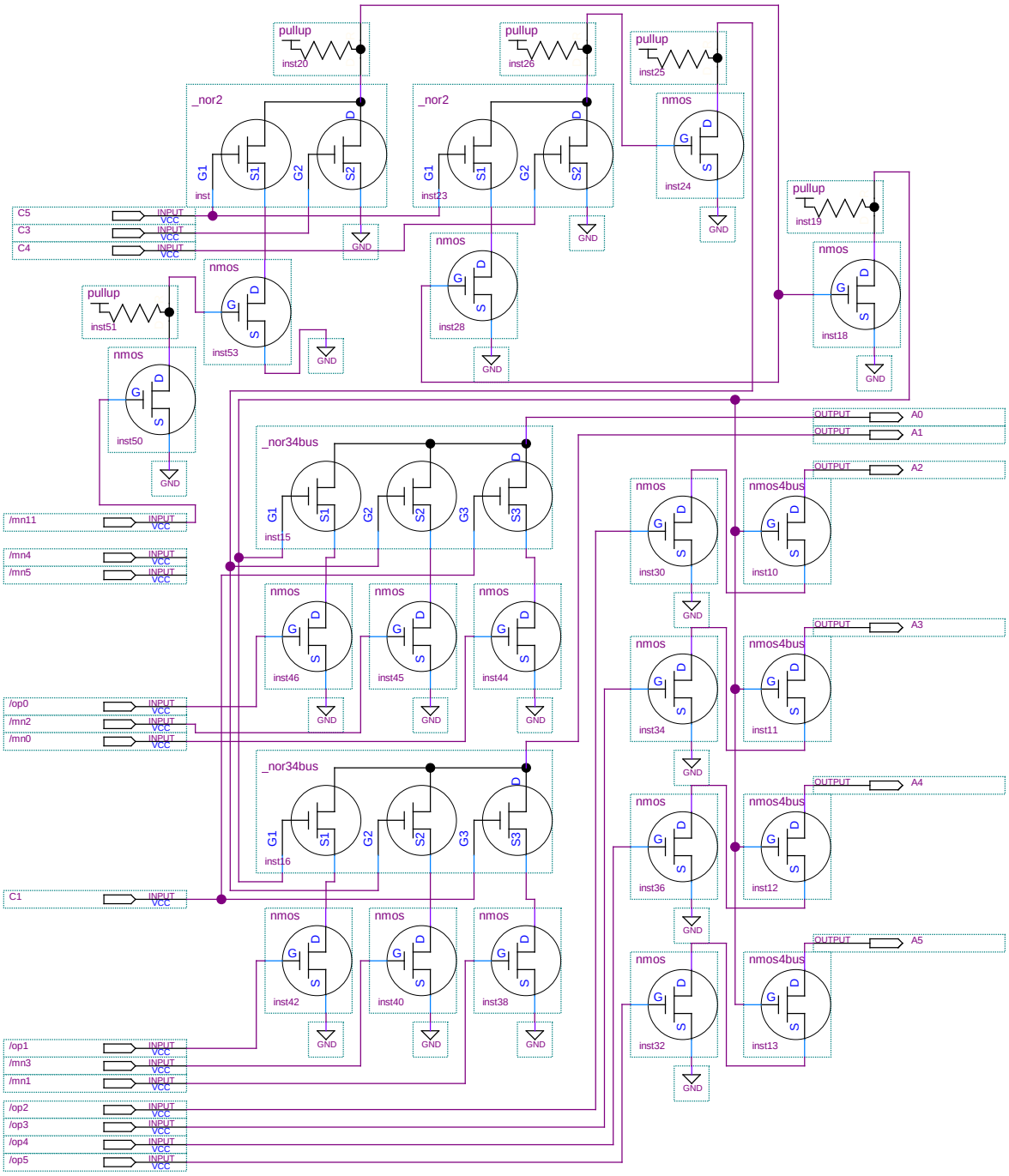

/CLK
CLK
RESET
LE
/LE
/D
/T
INPUT
VCC
_dff
D
/CLK
CLK
Q
RESET
/Q
inst
OUTPUT
Q
/Q
/COUT
pullup
inst7
inst9
inst10
inst22
_nor2
G1
S1
G2
S2
inst6
inst8
nmos
G
D
S
inst3
inst14
inst18
inst16
inst21
inst4
inst12
GND

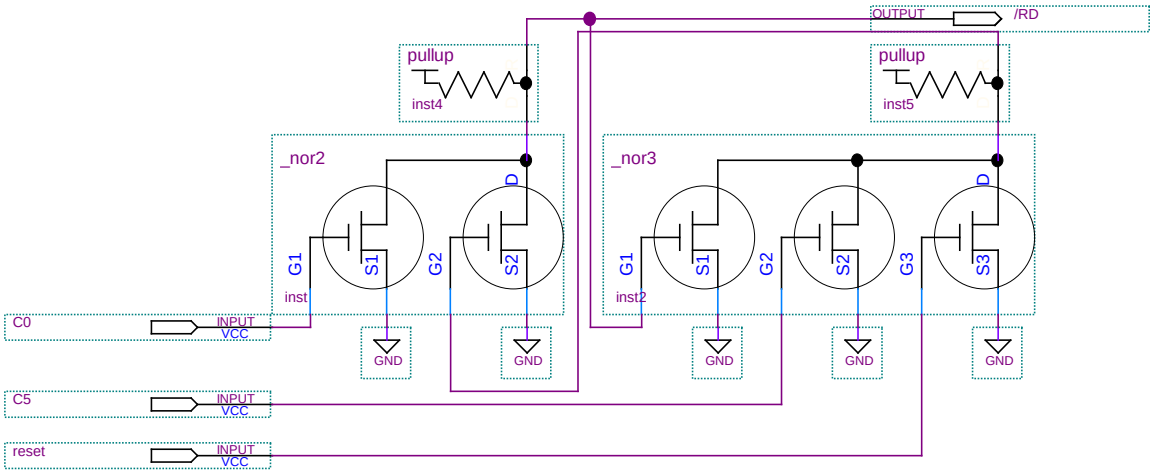

CLK
RESET
C0
C1
C2
C3
C4
C5
/L0
/L1
/L2
/L3
/L4
/L5

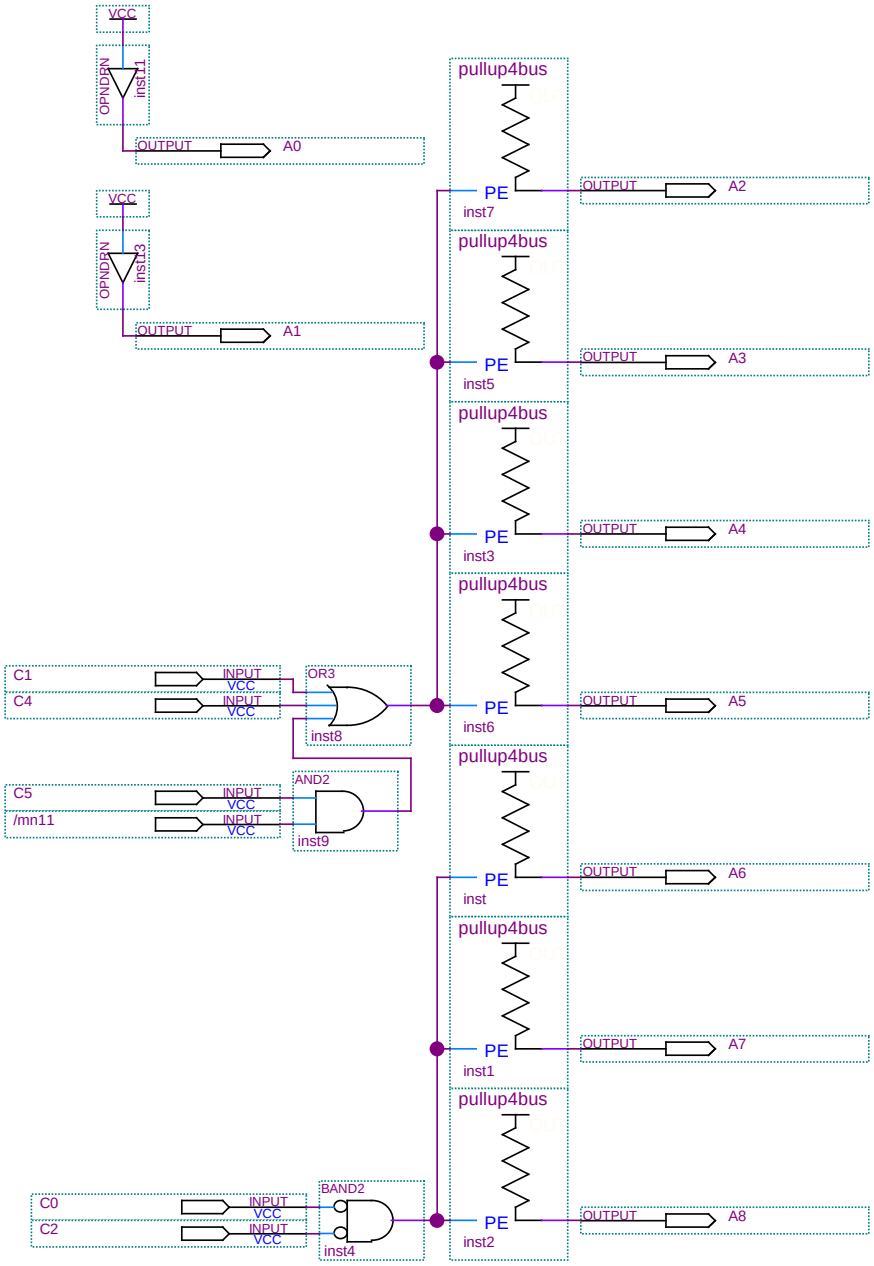

pullup
inst34
pullup
inst36
_nor2
inst31
nmos
inst35
nmos4bus
inst27
OUTPUT
A0
A1
A2
A3
A4
A5
A6
A7
A8
C2
C0
INPUT
VCC
GND
_tff2
/CLK
CLK
/LE
LE
/D
/T
Q
/Q
RESET
/COUT
inst10
inst9
inst8
inst7
inst6
inst5
inst4
inst3
inst11
inst13
inst30
inst2
inst16
inst17
inst41
inst40
inst43
inst39
inst46
inst19
inst60
inst20
inst58
inst21
inst56
inst22
inst54
inst23
inst52
inst24
inst50
inst25
inst44
inst26
inst48
/L4
D0
D1
D2
D3
D4
D5
BIDIR
/mn01
/mn2
/mn3
/mn4
/mn5
/op0
/op1
/op2
/op3
/op4
/op5
/mn0
/mn1
RESET


D0
D1
D2
D3
D4
D5
BIDIR
VCC
pullup
inst13
nmos
inst12
/L0
INPUT
GND
pullup
inst15
nmos
inst14
/L2
_dlatch
D
Q
LE
/Q
inst
inst1
inst2
inst3
inst4
inst5
inst6
inst7
inst8
inst9
inst10
inst11
OUTPUT
/mn0
/mn1
/mn2
/mn3
/mn4
/mn5
/op0
/op1
/op2
/op3
/op4
/op5
/mn11
/mn10
/mn01
/mn00
inst25
inst24
inst23
inst22
inst18
inst19
inst20
inst21
G
S




pullup
inst20
pullup
inst26
pullup
inst25
_nor2
inst
_nor2
inst23
nmos
inst24
pullup
inst19
nmos
inst18
C5
C3
C4
nmos
inst53
pullup
inst51
nmos
inst28
nmos
inst50
GND
_nor34bus
inst15
/mn11
/mn4
/mn5
nmos
inst46
nmos
inst45
nmos
inst44
/op0
/mn2
/mn0
_nor34bus
inst16
C1
nmos
inst42
nmos
inst40
nmos
inst38
/op1
/mn3
/mn1
/op2
/op3
/op4
/op5
INPUT
VCC
OUTPUT
A0
A1
A2
A3
A4
A5
nmos
inst30
nmos4bus
inst10
nmos
inst34
nmos4bus
inst11
nmos
inst36
nmos4bus
inst12
nmos
inst32
nmos4bus
inst13


OUTPUT
/RD
pullup
inst4
pullup
inst5
_nor2
_nor3
D
D
G1
S1
G2
S2
G1
S1
G2
S2
G3
S3
inst
inst2
C0
INPUT
VCC
GND
GND
GND
GND
GND
C5
INPUT
VCC
reset
INPUT
VCC


VCC
OPNDRN
inst11
OUTPUT
A0
VCC
OPNDRN
inst13
OUTPUT
A1
pullup4bus
PE
inst7
OUTPUT
A2
pullup4bus
PE
inst5
OUTPUT
A3
pullup4bus
PE
inst3
OUTPUT
A4
pullup4bus
PE
inst6
OUTPUT
A5
pullup4bus
PE
inst
OUTPUT
A6
pullup4bus
PE
inst1
OUTPUT
A7
pullup4bus
PE
inst2
OUTPUT
A8
C1
INPUT
VCC
C4
INPUT
VCC
OR3
inst8
C5
INPUT
VCC
/mn11
INPUT
VCC
AND2
inst9
C0
INPUT
VCC
C2
INPUT
VCC
BAND2
inst4